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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,953	12/31/2001	Chris Haywood	6979-0026	8426

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,953	HAYWOOD, CHRIS	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/31/2004 has been entered.

Response to Amendment

2. This Office action is in response to the amendment filed on 6/9/2004.

Claim Objections

3. Claim 4 is objected to because of the following informalities:

Claim 4 line 2, "number of blocks of having the selected block size" should be -- number of blocks of ***data*** having the selected block size--

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bass et al. (US PAT. 6,557,053 hereinafter Bass) in view of Shimizu (US PAT. 5,905,911).

Regarding claim 1, Bass discloses a caching system, i.e., a bandwidth conserving queue manager (10, figure 1) comprising a tail FIFO memory, i.e., input FIFO queue (14, figure 1) having a tail input to receive incoming frames (12, figure 1) from a outside source (col. 1 line 66 through col. 2 line 3), and a tail output to output the incoming frames, i.e., data (16, figure 1) is outputted from the input FIFO buffer 14 to a memory interface (18) and to a multiplexor (20) (col. 2 lines 3-5), a memory, i.e., memory (22) and memory interface (18), having a memory input, i.e., data(16) input to memory interface from input FIFO queue, and a memory output, i.e., output point from memory interface to multiplexor (20) as show in figure 1, the memory input is coupled to the tail output and the memory is operable to store data from the tail output, and wherein the memory is operable to output the stored data at the memory output (figure 2, col. 2 lines 14-36 and lines 45-51), a multiplexer (20, figure 1) having first multiplexer input, i.e., input direct from input FIFO queue (14) as show in figure 1, and a second multiplexer input, i.e., input from memory interface (18) as show in figure 1, the multiplexer having a control input, i.e., multiplexer control logic (24), to select one of the multiplexer inputs to coupled to a multiplexer output (col. 2 lines 7-12, 14-36 and col. 3 lines 35-52), a head FIFO memory, i.e., output FIFO queue (32, figure 1) having a head input coupled to the multiplexer output to receive data from the multiplexer output (figure 1), and a head output to output frames of the received data (col. 2 lines 7-12). Bass differs from the claimed invention in not specifically teaches the incoming frames containing varying amounts of data, and the caching system further comprising a

controller coupled to the tail FIFO, the head FIFO, and the memory and operable to transfer a dynamically selected number of blocks of data from the incoming frames having a dynamically selected block size from the tail FIFO to the memory and from the memory to the head FIFO, wherein the selected block size and the selected number of blocks together provide maximum memory transfer efficiency level. However, Shimizu teaches a data transfer system comprising a input device (1, figure 1) with a input FIFO (7, figure 1) and a output device (3, figure 1) with a output FIFO (8, figure 1), a direct memory access controller (5, figure 1), wherein the input device receives variable amount of data, i.e., one word or more, two words or more or four words or more (col. 5 lines 9-19), and the direct memory access controller further comprising a transfer count register (26) adapted to check whether or not all data in one block has been transferred, a size register (27) to temporarily hold a data transfer size output from a transfer size decision logic (30), to determines the data transfer size in accordance with the stored amount of input data to be output from the input device, and further determine a data transfer size in accordance with a buffer free space amount output from the output device (col. 3 line 42 through col. 5 line 49). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to the caching system of Bass in having the incoming frames containing varying amounts of data, and the caching system further comprising a controller coupled to the tail FIFO, the head FIFO, and the memory and operable to transfer a dynamically selected number of blocks of data from the incoming frames having a dynamically selected block size from the tail FIFO to the memory and from the memory to the head FIFO, wherein the selected block size and the selected number of blocks together provide maximum memory transfer efficiency level, as per teaching by the data transfer system of Shimizu, because it minimum of

bus transfer cycles, and significantly contributes to an increase of the speed and efficiency of data input/output in a computer system.

Regarding claim 2, Bass discloses the system wherein the head FIFO, i.e., output FIFO (32, figure 1) further comprises a head fill indicator coupled to the controller to indicate a fill characteristic of the head FIFO (col. 2 lines 21-32 and col. 3 lines 65 through col. 4 line 3).

Regarding claim 3, Bass discloses the system wherein the controller transfers the selected number of blocks of data having the selected block size from the input FIFO queue to the memory based on the output fill indicator (col. 2 lines 21-32, col. 3 line 65 through col. 4 line 3 and col. 4 lines 32-43).

Regarding claim 4, Bass discloses the system wherein the controller transfers the selected number of blocks of data having the selected block size from the memory to the head FIFO based on the head fill indicator (col. 2 lines 29-36 and col. 3 lines 41-51).

Regarding claim 5, Bass disclosures the system wherein the input FIFO queue further comprising a tail fill indicator, i.e., indicate the input FIFO queue is half full, empty, or completed full by writer pointer, read pointer and comparator (col. 2 line 66 through col. 3 line 12 and col. 3 line 53 through col. 4 line 3), coupled to the controller to indicated a fill characteristic of the input FIFO queue (col. 2 lines 24-36 and col. 3 lines 36-51).

Regarding claim 6, Bass discloses the system wherein the controller transfer the selected number of blocks of data having the selected block size from the tail FIFO to the memory based on the tail fill indicator (col. 2 lines 224-36, col. 3 lines 41-51 and col. 4 lines 32-43).

Regarding claim 7, Bass discloses the data comprises data frames of varying length and where the one or more blocks are defined to include data from one or more of the data frames,

and wherein a selected block may contain data from two or more data frames, i.e., the incoming data is fixed or selected size data, and the memory is able to reconstruct the oversize data when the amount of data being inputted exceeds the capacity or predetermined percentage of capacity of the input FIFO buffer and the output FIFO butter (col. 2 lines 32-65), in addition, Bass discloses the system further utilizes the head and tail pointers on contiguous addresses which further point out the edges the incoming data with selected size (col. 3 lines 23-33), furthermore, Bass discloses the incoming data width will be variable which based on the particular application (col. 4 line 18-27).

Regarding claim 8, Bass discloses the system wherein the controller includes a control output coupled to the control input of the multiplexer (figure 2), wherein the controller is operable to control which of the multiplexer inputs is coupled to the multiplexer output (col. 2 lines 7-12, lines 14-32 and col. 3 lines 35-51).

Regarding claim 9, Bass discloses the system wherein a data path to the memory is wider than a width characteristic of the input FIFO queue, i.e., the bus between input FIFO queue and output FIFO queue having the same width, and the data from input FIFO queue to the output FIFO is one data at a time, and the data from input FIFO queue to the memory (20) is three data items at a time (col. 2 line 67 through col. 3 line 11 and col. 4 lines 7-27).

Regarding claim 10, the limitations of the claim are rejected as the same reasons as set forth in claim 1.

Regarding claim 11, the limitations of the claim are rejected as the same reasons as set forth in claim 7.

Regarding claim 12, the limitations of the claim are rejected as the same reasons as set forth in claim 1.

Regarding claim 13, the limitations of the claim are rejected as the same reasons as set forth in claims 7-8.

Regarding claim 14, the limitations of the claim are rejected as the same reasons as set forth in claims 5-6.

Regarding claim 15, the limitations of the claim are rejected as the same reasons as set forth in claims 2-4.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stone et al. (US PAT. 6,389,489) disclosures data processing system having a FIFO buffer with variable threshold value based on input and output data rates and data block size (abstract).

Taylor (US PAT. 6,172,927) discloses FIFO integrated circuit memory device incorporating a retransmit function (col.2 line 63 through col. 3 line 57).

James et al. (US PAT. 5,845,145) discloses system for generating and sending a critical-word-first data response packet by creating response packet having data ordered in the order best matching the desired order (abstract).

Horikomi et al. (US PAT 6,687,768) discloses data stream generating apparatus and method of same, variable length coded data stream generation apparatus and method of same (abstract).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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